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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,710	12/05/2003	Yakov Belopolsky	FCI-2731/C3274A	4213

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EXAMINER	
BUI, HUNG S	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/729,710	BELOPOLSKY, YAKOV	
	Examiner	Art Unit	
	HUNG S. BUI	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 19* is/are allowed.

6)☒ Claim(s) *8-17,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/12/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8-11, 16-17 and 20-21 are rejected under 35 U.S.C.103(a) as being unpatentable over Dozier, II et al. in view of Chobot et al. [US 5,473,813].

Regarding claims 8-9 and 20-21, Dozier, II et al. disclose an electronic assembly, comprising a printed circuit board substrate (302, figure 3, column 22, line 23) including a retentive through hole (352, figures 3, column 26, line 11), a plurality of lands (306, figure 3), and an electrical connector (300, figure 3, column 23, lines 50-52), comprising:

- a housing (300, figure 3);

- a plurality of solder masses (314, figure 3, column 26, line 24) extending from a surface of the housing for electrically connecting the electrical connector to the land of the circuit substrate (figure 3);

- a retention structure (350, figure 3, column 26, line 11) extending from the surface of the housing, spaced apart from the plurality of solder masses (figure 3) and positioned within the thorough holes; and

- the retention structure having a cross-sectional area smaller than an area of the through hole so that a clearance exists between the retentive structure and a periphery of the through hole (figure 3).

Dozier, II et al. disclose the instant claimed invention except for the retention structure made with a material that is for combing with a solder composition within the through hole to affix the electrical connector to the circuit substrate at temperatures that initiate reflow of the plurality of solder masses.

Chobot et al. disclose an electronic assembly (figure 8) having a component mounted on a circuit substrate (S1-S4, figure 8) by a retentive structure; wherein the retentive structure comprises a mounting retentive pin (19, figure 8) and a retentive through hole (a through hole disposed in the circuit substrate of figure 8); the retention pin is inserted into the retentive through hole, being filled with solder composition material (21, figure 8), to affix the component on the circuit substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive structure design of Chobot et al. in Dozier II, et al., for the purpose of permanently mounting the housing socket onto the circuit substrate.

The melting temperature of the combination of the material and the solder composition being greater than the melting temperature of the solder masses, as well known in the art, it provides a soldering process.

Regarding claim 10-11, Dozier, II et al., as modified, disclose wherein the reflow temperature is various degrees.

Regarding claim 16, Dozier, II et al., as modified, disclose a plurality of solder masses (314, figure 3) extending from a surface of the housing for electrically connection to a circuit substrate (302, figure 3).

Regarding claim 17, Dozier, II et al. disclose an electronic assembly (figure 3), comprising:

- a housing (300, figure 3);

- a plurality of solder masses (314, figure 3, column 26, line 24) extending from a surface of the housing for electrically connecting the electrical connector to the land of the circuit substrate (figure 3); and

- a retention structure (350, figure 3, column 26, line 11) extending from the surface of the housing, spaced apart from the plurality of solder masses (figure 3) and positioned within the thorough holes; and

- the retention structure having a cross-sectional area smaller than an area of the through hole so that a clearance exists between the retentive structure and a periphery of the through hole (figure 3).

Dozier, II et al. disclose the instant claimed invention except for the retention structure made with a material that is for combing with a solder composition within the through hole to affix the electrical connector to the circuit substrate at temperatures that initiate reflow of the plurality of solder masses, such that the melting temperature of the combination of the material and the solder composition is greater than the melting temperature of the solder masses.

Chobot et al. disclose an electronic assembly (figure 8) having a component mounted on a circuit substrate (S1-S4, figure 8) by a retentive structure; wherein the retentive structure comprises a mounting retentive pin (19, figure 8) and a retentive through hole (a through hole disposed in the circuit substrate of figure 8); the retention

pin is inserted into the retentive through hole, being filled with solder composition material (21, figure 8), to affix the component on the circuit substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive structure design of Chobot et al. in Dozier II, et al., for the purpose of permanently mounting the housing socket onto the circuit substrate.

The melting temperature of the combination of the material and the solder composition being greater than the melting temperature of the solder masses, as well known in the art, it provides a soldering process.

7. Claims 13, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al., as modified, as applied to claim 9 above, and further in view of Melton et al. [US 5,086,966].

Regarding claims 13 and 15, Dozier, II et al., as modified, disclose the instant claimed invention except for the plating material/join being formed of palladinum.

Melton et al. disclose the use of palladinum in a solder composition for mounting an electrical component (column 1, line 65 - column 2, line 14).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use gold/palladinum with the solder composition of Dozier, II et al., as modified, as suggested by Melton et al., the purpose of improving solder wetting.

8. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dozier, II et al., as modified, as applied to claim 9 above, and further in view of Findeis et al. [US 6,203,690]

Regarding claims 12 and 14, Dozier, II et al., as modified, disclose the instant claimed invention except for the retentive structure is made with a base material and a plating material disposed over at least a portion of the base material.

Findeis et al. disclose a chip carrier (10, figures 1-3) having at least one retentive element (16) being mounted thereon, wherein the retentive element comprises a base material (Nickel layer 22) and a plating material (Gold layer 24) covered the base material (figures 1-3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the retentive element design of Findeis et al. for the retentive structure of Dozier, II et al., as modified, for the purpose of providing thermal conductivity between the socket/housing and the circuit board.

Allowable Subject Matter

3. Claims 1-7 and 19 are allowed.

Response to Arguments

4. Applicant's arguments with respect to claims 1-17 and 19-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Lauterbach et al. [US 5,029,748] disclose solder performs in a cast array.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung S. Bui whose telephone number is (571) 272-2102. The examiner can normally be reached on Monday-Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Hung S. Bui/
Primary Examiner, Art Unit 2841
7/20/2008